WE CLAIM:

1. A processor interface device, comprising:

at least one memory port, said at least one memory port adapted to transfer data and signals to and from a storage device;

at least one function port, said at least one function port adapted to transfer data and signals to and from a macro function;

a data transfer fabric adapted to transfer data and signals between said at least one memory port and said at least one function port, and

an arbitration unit adapted to arbitrate access to various portions of said memory by said macro function.

2. The processor interface device of Claim 1, wherein said data transfer fabric comprises a crossbar switch fabric.

3. The processor interface device of Claim 1, further comprising a macro function in data communication with said at least one function port, said macro function being controlled at least in part by a processor instruction associated with said macro function, wherein said macro function may access said at least one memory port.

4. The processor interface device of Claim 1, further comprising a plurality of macro functions in data communication with respective ones of said function ports, said interface device further adapted to allow simultaneous access of multiple ones of said memory ports by respective ones of said macro functions via said function ports.

5. The processor interface device of Claim 4, wherein said at least one of said macro functions is controlled by at least one processor instruction associated with an instruction set of a parent processor.

6. The processor interface device of Claim 5, wherein said parent processor comprises an extensible RISC processor, and said instruction set comprises an extended instruction set thereof.

7. The processor interface device of Claim 5, wherein said data transferred from said storage device via said interface device is processed in pipeline fashion by at least two of said plurality of macro functions.

8. The interface device of Claim 7, wherein said act of processing in pipeline fashion comprises;

assigning each of said at least two macro functions as particular stages in a pipeline; and

sequentially processing said data in said stages of said pipeline.

9. A processing device, comprising:

a first data processor having an instruction set associated therewith;

a second data processor adapted to process data in a predetermined manner;

a memory array having at least one memory bank, said at least one memory bank being adapted to store a plurality of data;

a memory interface, said memory interface having at least one first port adapted for data communication between said interface and said memory array, and at least one second port adapted for data communication between said interface and said second processor;

wherein access to said memory array via said at least one memory port is controlled at least in part by said second data processor.

10. The device of Claim 9, further comprising an arbitration unit which arbitrates access to said at least one memory bank during said access to said memory array.

11. The device of Claim 9, wherein said at least one function port further comprises at least one function controller having a plurality of registers.

12. The device of Claim 11, wherein said plurality of registers comprises registers selected from the group comprising control, status, and test registers.

13. The device of Claim 11, wherein said at least one function controller further comprises an interface to at least one pipeline stage of said first data processor.

14. The device of Claim 9, further comprising a crossbar adapted for data communication between said at least one memory port and said at least one function port.

15. The device of Claim 14, wherein said crossbar permits simultaneous access to each of said at least one memory ports by at least one of said at least one function ports.

16. The device of Claim 9, wherein said second data processor comprises a digital signal processor, said digital signal processor being optimized for calculation based on at least one predetermined algorithm.

17. The device of Claim 9, wherein said second data processor comprises an application specific integrated circuit (ASIC).

18. A method of accessing data disposed within a plurality of memory banks, comprising;

providing at least first and second macro functions adapted to process data;

providing a memory interface having at least two function ports and two memory ports, each of said memory ports being in data communication with respective ones of said memory banks, each of said function ports being capable of data communication with each of said memory ports, said first and second macro functions being in data communication with respective ones of said at least two function ports;

controlling the operation of said first and second macro functions using at least one parent processor instruction; and

simultaneously accessing said data disposed with in respective ones of said memory banks using respective ones of said macro functions.

19. The method of Claim 18, further comprising arbitrating access to said at least two memory ports by said at least first and second function ports using a crossbar.

20. The method of Claim 18, wherein the act of controlling comprises initiating at least one of said first and second macro functions using an instruction decoded in the instruction decode stage of the parent processor.

21. The method of Claim 20, wherein the act of controlling further comprises controlling at least one of said macro functions based at least in part on one immediate (imm) operand derived from said decoded instruction.

22. The method of Claim 18, wherein the act of controlling comprises accessing at least one extension register resident within said parent processor.

23. A method of testing a function associated with a parent processor and memory interface having a plurality of registers and being adapted for data communication between a memory array and said function, said method comprising:

providing a test sequence adapted to test said function;

providing an input test value within said memory array;

initiating said function;

generating results from said function based on said input test value; and

comparing said results to a known value.

24. The method of Claim 23, further comprising duplicating a control value in at least one of said registers.

25. A processing device, comprising:

first means for processing data, said first means for processing having an instruction set associated therewith;

second means for processing data, said second means being adapted to process data in a predetermined manner;

memory means having at least one memory bank, said at least one memory bank being adapted to store a plurality of data;

interface means, said interface means having at least one first port adapted for data communication between said interface means and said memory means, and at least one second port adapted for data communication between said interface means and said second means for processing;

wherein access to said memory means via said at least one memory port is controlled at least in part by said second means for processing.

26. A method of generating a design for an integrated circuit device comprising at least one processor core, memory interface with at least one memory port and function port, and macro function, comprising;

editing a first file specific to the design;

providing at least one library file, said at least one library file including information regarding said at least one memory interface and macro function;

generating a script based at least in part on said first file, said at least one library file, and input obtained from a designer;

running said script to create a description language model of said device; and

generating said design based at least in part on said description language model.

27. The method of Claim 26, wherein the act of generating further comprises specifying data communication between said at least one macro function and said function port of said at least one memory interface.

28. The method of Claim 27, wherein the act of generating further comprises specifying control of at least a portion of said at least one macro function by at least one instruction with the instruction set of said processor core.

29. The method of Claim 26, wherein said at least one macro function is "soft", and the act of generating further comprises adapting said at least one soft macro function to the specifications of said memory interface.

30. A processor interface device, comprising:

at least one memory port, said at least one memory port adapted to transfer data and signals to and from a data storage means;

at least one function port, said at least one function port adapted to transfer data and signals to and from a means for performing a processing function;

means for transferring data and signals between said at least one memory port and said at least one function port, and

arbitration means for arbitrating access to various portions of said memory by said means for performing.